Code No: D0603, D7704, D5704 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
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DESIGN OF FAULT TOLERANT SYSTEMS
(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1. What is the primary goal of fault tolerance? Define the reliability of a system. What property of a system the reliability characterizes? In which situations is high reliability required? What is the difference between the reliability and the availability of a system? How does the point availability compare to the system's reliability if the system cannot be repaired? What is the steady-state availability of a non repairable system? [12]

2. You are provided with five modules of the same type to design a fault-tolerant system. You have several possible choices to organize redundancy. The Unreliability of the modules, a five input majority voter, a three input majority voter, a 2 to 1 selection circuit, and a 2 input comparator are URm, UR5, UR3, UR2s, and UR2c, respectively. Design at least three different configurations to arrange redundancy using all five modules and rank order them according to their expected reliability. Assume UR5 = 2 * UR3, UR3 = 2 * UR2s, and UR2s = UR2c. Make any reasonable assumption if you need to simplify your expressions.
Note: There is no need to use all the connecting logics (voters, comparator, and selection circuit) in a given configuration. [12]

3. Suppose that the reliability of a system consisting of 4 blocks, two of which are identical, is given by the following equation: Rsystem = R1R2R3 + (R1power) 2 – (R 1power) 2 *R2*R3. Draw the reliability block diagram representing the system. [12]

4. Explain Berger code for a totally self checking checker. Information bits I= 0101000 , calculate check bits , and berger code. Design a totally self checking checker, for the information bits. [12]

5. Design a Totally self checking PLA for the equation
$z1 = x1x2 + x1'x2'$

$z2 = x1'x2$ [12]

Contd…..2

6. Derive for the following expression

$$F = x_1x_2x_3x_4 + x_1x_2x_3x_4 + x_1x_2x_3x_4 + x_1x_2x_3x_4 + x_1x_2x_3x_4 + x_1x_2x_3x_4 + x_1x_2x_3x_4 + x_1x_2x_3x_4$$

   a. Reed-Muller expansion
   b. Design the circuit for the Reed-Muller expansion implementation. [12]

7. Explain Scan design requirements, design a combinational scan structure with FF's, such a way that the structure can be fully tested by compact ATPG patterns. [12]

8. Explain in detail Pseudo random testing, Given n and k , then T exhaustively covers all binary k – subspaces If it contains all binary n-tuples of weights w such that w= c mod (n-k+1) for some integer constant c, where 0<= c<=n-k. LET Tc denote the set produced from the above assumption. For specific value of c. solve the statement for n=20, k=2, n-k+1=19. [12]

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